



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,116	12/06/2001	Mark Tuttle	M4065.0363/P363-A	5771

24998 7590 10/04/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER

BEREZNY, NEMA O

ART UNIT	PAPER NUMBER
----------	--------------

2813

DATE MAILED: 10/04/2002

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/003,116

Applicant(s)

TUTTLE, MARK

Examiner

Nema O Berezny

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 70-96 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 70-96 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 90 recites the limitation "said printed circuit board" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 70 is rejected under 35 U.S.C. 102(b) as being anticipated by Sudoh et al. (5,352,925). Sudoh discloses a method of packaging a semiconductor device,

Art Unit: 2813

comprising: electrically coupling (Fig.4 el.2) a die carrier (el.1) to a first surface of a die (el.6); and contacting a second surface of said die with a first layer of magnetic field shielding material (el.3) which shields said die from external magnetic fields (col.3 line 66 – col.4 line 21).

Claims 87-88 and 90 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (4,801,489). Nakagawa discloses a method of forming a chip carrier, comprising: forming an insulating layer (Fig.8 el.24) over a first surface of a substrate (el.12); inherently providing a support surface for an integrated circuit chip; and providing a layer of magnetic field shielding material (el.22,26) between said insulating layer and said first surface, and on the top and bottom surfaces of said substrate, which shields said IC chip from external magnetic fields.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 71-74 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudoh as applied to claim 70 above, and further in view of Nakagawa et al. (4,801,489). Sudoh does not disclose mounting said die carrier to a printed circuit board. However, Nakagawa discloses forming a printed circuit board, PCB (Fig.10

Art Unit: 2813

el.12) which has a second layer of magnetic field shielding material (el.22,26; title; col.18 lines 9-15) formed on a top and bottom surface of said PCB. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the printed circuit board of Nakagawa with the method of packaging a semiconductor device of Sudoh. Sudoh discloses in Fig.12 that the shielded device on a substrate is ultimately mounted and electrically coupled to a PCB (el.30; col.5 lines 50-53). Adkins (4,408,255) discloses a package comprising integrated circuits with a shielded layer mounted to a PCB which is also shielded (Fig.4A), wherein the advantages comprise: reducing the electromagnetic interference (EMI) field from reaching other components within the originating circuit (the upper shield layer), and reducing EMI from propagating out through connectors and cables (the lower shield layer) – (col.4 line 50 – col.5 line 7).

Claim 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sudoh in view of Nakagawa as applied to claims 70-74 above, and further in view of Fukuoka (5,949,654). Sudoh in view of Nakagawa do not disclose a magnetic field shielding material embedded within a PCB. However, Fukuoka discloses a multiple layered PCB, comprising an embedded magnetic shielding material layer (Fig.1 el.104). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the embedded magnetic shielding material layer of Fukuoka with the method of packaging a semiconductor device of Sudoh in view of Nakagawa in order to be able to attach external terminals to said PCB.

Claim 89 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa as applied to claims 87-88 above, and further in view of Fukuoka (5,949,654). Nakagawa does not disclose a magnetic field shielding material embedded within a PCB. However, Fukuoka discloses a multiple layered PCB, comprising an embedded magnetic shielding material layer (Fig.1 el.104). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the embedded magnetic shielding material layer of Fukuoka with the method of packaging a semiconductor device of Nakagawa in order to be able to attach external terminals to said PCB.

Claims 77-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudoh in view of Nakagawa as applied to claims 70-74 and 76 above, and further in view of Tracy et al. (5,902,690). Sudoh in view of Nakagawa do not disclose a magnetic memory device or shielding material comprising ferrites, manganites, chromites or cobaltites. However, Tracy discloses forming a magnetic RAM device (title), and first layer magnetic field shielding material comprising nickel ferrite (col.4 line 65 – col.5 line 10), and magnetic material comprising nickel particles (col.5 lines 15-30). It would have been obvious to a person of ordinary skill in the semiconductor art to also use the nickel ferrite and nickel ferrite particles for the second magnetic field shielding material. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the MRAM device of Tracy with the method of packaging

Art Unit: 2813

a semiconductor device of Sudon in view of Nakagawa in order to effectively shield said device from undesirable magnetic fields. Adkins (4,408,255) discloses a package comprising integrated circuits with a shielded layer mounted to a PCB which is also shielded (Fig.4A), wherein the advantages comprise: reducing the electromagnetic interference (EMI) field from reaching other components within the originating circuit (the upper shield layer), and reducing EMI from propagating out through connectors and cables (the lower shield layer) – (col.4 line 50 – col.5 line 7).

Claims 91-96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa as applied to claims 87, 88, and 90 above, and further in view of Tracy et al. (5,902,690). Nakagawa does not disclose a magnetic memory device or shielding material comprising ferrites, manganites, chromites or cobaltites. However, Tracy discloses forming a magnetic RAM device (title), and magnetic field shielding material comprising nickel ferrite (col.4 line 65 – col.5 line 10), and magnetic material comprising nickel particles (col.5 lines 15-30). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the MRAM device of Tracy with the method of packaging a semiconductor device of Nakagawa in order to effectively shield said device from undesirable magnetic fields. Adkins (4,408,255) discloses a package comprising integrated circuits with a shielded layer mounted to a PCB which is also shielded (Fig.4A), wherein the advantages comprise: reducing the electromagnetic interference (EMI) field from reaching other components within the originating circuit

Art Unit: 2813

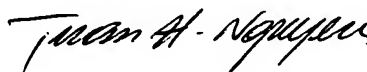
(the upper shield layer), and reducing EMI from propagating out through connectors and cables (the lower shield layer) – (col.4 line 50 – col.5 line 7).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (703) 305-3445. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



NB
October 1, 2002

Tuan H. Nguyen
Primary Examiner